REMARKS

Prior to the present response, claims 1, 3, 6, 9-10, 13, 15, 19, and 21 were pending in the present application, and remain in the present application after the present response. Reconsideration and allowance of pending claims 1, 3, 6, 9-10, 13, 15, 19, and 21 in view of the following remarks are requested.

At the outset, it is noted that in the Office Action dated March 24, 2009, the Examiner has ***finally rejected*** claims 1, 3, 6, 9-10, 13, 15, 19, and 21 pending in the application on the basis of new ground(s) of rejection and newly cited art. Applicants respectfully request reconsideration and withdrawal of the finality of the rejection of the Office Action dated June 5, 2009.

A good and sufficient reason why the present response is necessary and was not earlier presented is that a new reference has been cited in the present final rejection dated June 5, 2009. The new reference is U.S. patent number 6,803,266 B2 to Solomon et al. (hereinafter "Solomon"). Since Solomon is a new reference upon which the Examiner has now relied, Applicants believe that it would be manifestly unfair for the Patent Office not to withdraw the finality of the present rejection and not to consider Applicants' arguments which are necessitated due to the newly cited reference, Solomon. As such, a good and sufficient reason exists, as contemplated by 37 CFR §1.116(c), for withdrawing the finality of the present rejection.

A. **Rejection of Claims 1, 3, 15, and 19 under 35 USC §102(e)**

The Examiner has rejected claims 1, 3, 15, and 19 under 35 USC §102(e) as being anticipated by Solomon. For the reasons discussed below, Applicants respectfully submit that the present invention, as defined by independent claims 1 and 15, is patentably distinguishable over Solomon.

The present invention, as defined by independent claim 1, provides a FET including a first gate dielectric having a first coefficient of thermal expansion and a first gate electrode having a second coefficient of thermal expansion, where the first gate electrode and the first gate dielectric are selected such that said second coefficient of thermal expansion is greater than said first coefficient of thermal expansion so as to cause an increase in carrier mobility in the channel. In one embodiment of the present invention as shown in Figure 1 of the present application, FET 102 includes source 108, drain 110, channel 112, gate electrode layer 114, and gate dielectric layer 116, where channel 112 is situated in substrate 104 between source 108 and drain 110, gate dielectric layer 116 overlies channel 112, and gate electrode layer 114 overlies gate dielectric layer 116. *See*, e.g., Figure 1 and related text of the present application. For example, gate dielectric layer 116 can have a thickness of between 10.0 Angstroms and 15.0 Angstroms. *See*, e.g., page 7, lines 1-2 of the present application.

As disclosed in the present application, gate electrode layer 114 and gate dielectric layer 116 are selected such that gate electrode layer 114 has a coefficient of thermal expansion (CTE) that is higher than a CTE of gate dielectric layer 116. *See*, e.g., page 7, lines 7-9 of the present application. As a result, as a wafer comprising structure 100

cools down after gate electrode layer 114 has been deposited at high temperature, gate electrode layer 114 decreases in size to a greater extent (i.e. shrinks more) than gate dielectric layer 116, thereby creating tensile strain in channel 112, which advantageously increases carrier mobility in channel 112. *See*, e.g., page 7, lines 9-13 of the present application. In an embodiment in which FET 102 is a PFET, gate dielectric layer 116 and gate electrode layer 114 are selected such that gate dielectric layer 116 has a higher CTE than gate electrode layer 114, which advantageously increases carrier mobility in channel 112 by creating compressive strain in the channel. *See*, e.g., page 7, lines 13-17 and Figure 1 of the present application.

In contrast to the present invention as defined by independent claim 1, Solomon does not disclose a FET including a first gate dielectric having a first coefficient of thermal expansion and a first gate electrode having a second coefficient of thermal expansion, where the first gate electrode and the first gate dielectric are selected such that said second coefficient of thermal expansion is greater than said first coefficient of thermal expansion so as to cause an increase in carrier mobility in the channel. Solomon is directed to a process for passivating the semiconductor-dielectric interface of a MOS structure to reduce the interface state density to a very low level. *See*, e.g., the Abstract of Solomon. Solomon specifically discloses MOSFET device 10 including semiconductor substrate 12, a pair of wells 14 that serve as the source and the drain of device 10, gate dielectric 16 overlying channel 20 between the source and drain wells 14, and gate electrode 18 overlying gate dielectric 16. *See*, e.g., column 3, lines 44-48 and Figure 1 of Solomon. In Solomon, gate dielectric 16 can have a thickness of about 5 nm

(50 Angstroms) or less for a silicon dioxide gate dielectric, and a thickness of about 20 nm (200 Angstroms) or less for other gate dielectric materials. *See*, e.g., column 4, lines 13-17 of Solomon.

Solomon discloses that although silicon dioxide is a preferred material for gate dielectric 16, it is foreseeable that other dielectric materials could be used, such as high-k dielectrics including Y_2O_3, La_2O_3, Al_2O_3, ZnO_2, HfO_2, and mixtures thereof. *See*, e.g., column 3, lines 58-62 of Solomon. Solomon also discloses that a preferred material for gate electrode 18 is tungsten, though other suitable gate electrode materials include tungsten and cobalt silicides and tantalum nitride. *See*, e.g., column 4, lines 7-10 of Solomon. As further disclosed in Solomon, "the present invention is generally applicable to gate electrodes formed of essentially any metal that renders the electrode 18 impermeable to molecular hydrogen." *See* column 4, lines 10-13 of Solomon.

However, Solomon fails to disclose a FET including a first gate dielectric having a first coefficient of thermal expansion and a first gate electrode having a second coefficient of thermal expansion, where the first gate electrode and the first gate dielectric are selected such that said second coefficient of thermal expansion is greater than said first coefficient of thermal expansion so as to cause an increase in carrier mobility in the channel, as specified in independent claim 1. In fact, Solomon does not even mention the coefficient of thermal expansion of either gate dielectric 16 or gate electrode 18.

In the outstanding Final Rejection, the Examiner asserts:

> It is noted that the first gate dielectric (16) is made of silicon dioxide and the first gate electrode (18) made of tungsten (col. 3, lines 57-60 and col. 4, lines 12-15). The coefficients of thermal expansion of silicon dioxide

> and tungsten are $2.3X10^{-6}$ /K (paragraph [0084] of U.S. Publication No. 2008/0278787, provided herein as evidence only) and $4.5X10^{-6}$ /K (paragraph [0043], U.S. Publication No. 2009/0099553, provided herein as evidence only) respectively. Therefore, the second coefficient of thermal expansion is greater than the first coefficient of thermal expansion so as to cause an increase in carrier mobility in said FET channel since the difference in the first coefficient of thermal expansion and the second coefficient of thermal expansion inherently causes an increase in carrier mobility in said FET. *See* pages 2 and 3 of the Final Rejection dated June 5, 2009.

Applicants do not dispute the teachings of U.S. Publication No. 2008/0278787 and U.S. Publication No. 2009/0099553. However, independent claim 1 specifies that the first gate electrode and the first gate dielectric are selected such that said second coefficient of thermal expansion is greater than said first coefficient of thermal expansion so as to cause an increase in carrier mobility in the channel.

As disclosed in the present application, this relationship is (by implication) true for an NFET. However, for a PFET, carrier mobility is increased in the channel when the first coefficient of thermal expansion (e.g. the CTE of gate dielectric layer 116) is greater than the second coefficient of thermal expansion (e.g. the CTE of gate electrode layer 114) so as to cause a compression strain in the channel. *See*, e.g., page 7, lines 13-17 of the present application. Thus, whether the FET is an NFET or a PFET determines the required relationship between CTE of the gate electrode and the CTE of the gate dielectric to cause an increase in carrier mobility in the channel. However, the distinction between the type of strain (i.e. tensile strain or compressive strain) produced in the channel to cause an increase in carrier mobility and the type of FET (i.e. NFET or PFET)

is not disclosed in Solomon or in U.S. Publication Nos. 2008/0278787 and 2009/0099553, which the Examiner provides as evidence only.

For all the foregoing reasons, Applicants respectfully submit that, at the time the invention defined by independent claim 1 was made, the invention would not have been obvious to a person of ordinary skill in the art by Solomon. Thus, independent claim 1 is patentably distinguishable over Solomon and, as such, claim 3 depending from a independent claim 1 is, *a fortiori*, also patentably distinguishable over Solomon for at least the reasons presented above and also for additional limitations contained in the dependent claim.

The present invention, as defined by independent claim 15, requires a first gate dielectric having a first coefficient of thermal expansion and a first gate electrode having a second coefficient of thermal expansion, where the first gate electrode and the first gate dielectric are selected such that said first coefficient of thermal expansion is greater than said second coefficient of thermal expansion so as to cause an increase in carrier mobility in the channel, and where the FET is a PFET. For similar reasons as discussed above, Applicants respectfully submit that, at the time the invention defined by independent claim 15 was made, the invention would not have been obvious to a person of ordinary skill in the art by Solomon. As such, independent claim 15 is patentably distinguishable over Solomon. Thus, claim 19 depending from independent claim 15 is, *a fortiori*, also patentably distinguishable over Solomon for at least the reasons presented above and also for additional limitations contained in the dependent claim.

B. Rejection of Claims 6, 9, 10, 13, and 21 under 35 USC §103(a)

The Examiner has rejected claims 6, 9, 10, 13, and 21 under 35 USC §103(a) as being unpatentable over Solomon. As discussed above, independent claims 1 and 15 are patentably distinguishable over Solomon. Thus claim 6 depending from independent claim 1 and claim 21 depending from independent claim 15 are, *a fortiori*, also patentably distinguishable over Solomon for at least the reasons presented above and also for additional limitations contained in each dependent claim.

Independent claim 9 defines similar subject matter as independent claim 1, with a difference being that independent claim 9 specifies that the first gate dielectric has a thickness of between 10.0 Angstroms and 15.0 Angstroms. As discussed above, Solomon discloses a gate dielectric (e.g. gate dielectric 16) having a thickness of about 5 nm (50 Angstroms) or less for a silicon dioxide gate dielectric, and a thickness of about 20 nm (200 Angstroms) or less for other gate dielectric materials. Thus, Solomon discloses a gate dielectric thickness that is substantially greater than the gate dielectric thickness specified in independent claim 9. Thus, for all of the reasons discussed above, independent claim 9 is also patentably distinguishable over Solomon. As such, claims 10 and 13 depending from independent claim 9 are also patentably distinguishable over Solomon for at least the reasons presented above and also for the additional limitations contained in each dependent claim.

C. Conclusion

For all the foregoing reasons pending claims 1, 3, 6, 9-10, 13, 15, 19, and 21 are patentably distinguishable over the cited art, and an early allowance of pending claims 1, 3, 6, 9-10, 13, 15, 19, and 21 is respectfully requested.

The Commissioner is hereby authorized to charge payment of any additional fees associated with this communication, or credit any overpayment to Deposit Account No. 50-0731.

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Respectfully Submitted,
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